COMPLETE SET OF PENDING CLAIMS

1. (Previously Presented) A thin film transistor array panel comprising:

a gate line and a data line formed on an insulating substrate and intersecting each other;

a plurality of common electrodes separated from the gate line and the data line and making an angle of about 7-23 degrees with the gate line;

a plurality of pixel electrodes separated from the gate line, the data line, and the common electrodes, extending parallel to the common electrodes, and alternately arranged with the common electrodes; and

a thin film transistor connected to the gate line, the data line, and the pixel electrodes,

wherein the distance between a one of the plurality of common electrodes and an adjacent one of the plurality of pixel electrodes is greater than the respective width of the one of the plurality of common electrodes and the adjacent one of the plurality of pixel electrodes.

2. (Previously presented) The thin film transistor array panel of claim 1, wherein the common electrodes include first and second electrodes making an angle of about 15-45 degrees with each other.

3. (Original) The thin film transistor array panel of claim 1, further comprising a connecting electrode connecting the common electrodes and a common electrode line extending parallel to the gate line and connected to the connecting electrode.

4. (Original) The thin film transistor array panel of claim 1, further comprising a pixel electrode line

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connecting the pixel electrodes and extending parallel to the data lines.

5. (Previously Presented) A thin film transistor array panel comprising:

an insulating substrate;

a gate line formed on the insulating substrate;

a common electrode line including a plurality of branched common electrodes making an angle of about 7-23 degrees with the gate line;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed at least in part on the semiconductor layer;

a pixel electrode line formed at least in part on the semiconductor layer and including a plurality of branched pixel electrodes alternately arranged with the common electrodes; and

a passivation layer formed on the data line and the pixel electrode line,

wherein the distance between the one of the plurality of branched common electrodes and an adjacent one of the plurality of branched pixel electrodes is greater than the respective width of the one of the plurality of branched common electrodes and the adjacent one of the plurality of pixel electrodes.

6. (Original) The thin film transistor array panel of claim 5, wherein the common electrodes comprise first and second electrodes making an angle of about 15-45 degrees with each other.

7. (Original) The thin film transistor array panel of claim 6, wherein the pixel electrodes comprise third

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and fourth electrodes extending parallel to the first and the second electrodes, respectively.

8. (Previously presented) The thin film transistor array panel of claim 5, further comprising a redundant data line formed on the passivation layer and extending along the data line, the passivation layer having a contact hole for connection between the data line and the redundant data line.

9. (Original) The thin film transistor array panel of claim 5, further comprising a contact assistant formed on the passivation layer, the passivation layer having a contact hole exposing a portion of the data line and covered by the contact assistant.

10. (Original) The thin film transistor array panel of claim 5, wherein the common electrode line extends substantially parallel to the gate line and further includes a frame connecting the common electrodes.

11. (Original) The thin film transistor array panel of claim 5, wherein the pixel electrode line extends substantially parallel to the data line.

12. (Original) The thin film transistor array panel of claim 5, further comprising an ohmic contact disposed between the semiconductor layer and the data line and the pixel electrode line.

13. (Original) The thin film transistor array panel of claim 12, wherein the semiconductor layer has substantially the same planar shape as the data line and the pixel electrode line and the ohmic contact.

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14. (Previously Presented) A liquid crystal display comprising:

a first substrate;

a gate line and a data line formed on the first substrate and intersecting each other;

a plurality of common electrodes separated from the gate line and the data line and making an angle of about 7-23 degrees with the gate line;

a plurality of pixel electrodes separated from the gate line, the data line, and the common electrodes, extending parallel to the common electrodes, and alternately arranged with the common electrodes;

a thin film transistor connected to the gate line, the data line, and the pixel electrodes;

a second substrate; and

a liquid crystal layer interposed between the first substrate and the second substrate,

wherein the distance between a one of the plurality of common electrodes and an adjacent one of the plurality of pixel electrodes is greater than the respective width of the one of the plurality of common electrodes and the adjacent one of the plurality of pixel electrodes.

15. (Previously presented) The thin film transistor array panel of claim 1, further comprising a redundant data line formed on the passivation layer and extending along the data line, the passivation layer having a contact hole for connection between the data line and the redundant data line,

wherein the redundant data line is made of a material selected from the group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), and chromium (Cr).

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16. (Previously presented) The thin film transistor array panel of claim 8, wherein the redundant data line is made of a material selected from the group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), and chromium (Cr).

17. (Previously presented) The thin film transistor array panel of claim 14, further comprising:

a redundant data line formed on a passivation layer and extending along the data line, the passivation layer having a contact hole for connection between the data line and the redundant data line, the redundant data line and the data line being connected through the contact hole,

wherein the redundant data line is made of a material selected from the group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), and chromium (Cr).

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